CLAIM AMENDMENTS

1. (Cancelled)

2. (Currently Amended) ~~The word current source of claim 1~~ A word current source for a magnetoresistive random access memory circuit comprising, in combination:

a control circuit having a control input;

an n-channel transistor including a gate, a source and a drain, where the source is coupled to a supply ground, the drain is coupled to the magnetoresistive random access memory circuit and the gate is connected to the control input; and

a positive supply voltage coupled to the magnetoresistive random access memory circuit so as to allow current to flow through the magnetoresistive random access memory circuit when an activation signal is applied to the gate by the control circuit;

wherein the control circuit comprises a voltage regulator that regulates a voltage level at the gate, so as to limit an amount of current flowing through the n-channel transistor and the magnetoresistive random access memory circuit.

3. (Original) The word current source of claim 2 with the voltage regulator comprising a feed back amplifier.

4. (Original) The word current source of claim 2 with the voltage regulator being current controlled.

5. (Currently Amended) The word current source of claim [[1]] 2 with the n-channel transistor comprising a complementary metal oxide semiconductor n-channel field effect transistor.

6. (Original) The word current source of claim 5 wherein the control circuit comprises a current regulator that regulates current flowing through the complementary metal

oxide semiconductor (CMOS) n-channel field effect transistor when the CMOS n-channel field effect transistor is turned on and off.

7. (Original) The word current source of claim 6 with the current regulator comprising a feed-back amplifier.

8. (Cancelled).

9. (Currently Amended) ~~The word current source of claim 8 with the stabilization amplifier further comprising, in combination:~~ A word current source for a magnetoresistive random access memory circuit comprising, in combination:

a control circuit having a control input;

an n-channel transistor including a gate, a source and a drain, where the source is coupled to a supply ground, the drain is coupled to the magnetoresistive random access memory circuit and the gate is connected to the control input; and

a positive supply voltage coupled to the magnetoresistive random access memory circuit so as to allow current to flow through the magnetoresistive random access memory circuit when an activation signal is applied to the gate by the control circuit.

wherein the control circuit comprising a stabilization amplifier, comprising:

a logic control having a read/write input and an on/off input and a write reference gate control signal and a read reference gate control signal;

a read reference switch having a read reference input and a reference output, with the read reference switch having a read reference control connected to the read reference gate control signal;

a write reference switch having a write reference input and a write reference output connected to the reference output, with the write reference switch having a write reference control connected to the write reference gate control signal; and

a feedback amplifier connected to the reference output, having a mirror current output and a mirror feedback voltage input.

10. (Cancelled)

11. (Original) A word current source for a magnetoresistive random access memory circuit comprising, in combination:

a control circuit having a regulated mirror gate signal;

a complementary metal oxide semiconductor (CMOS) n-channel transistor including a gate, a source and a drain, where the source is coupled to a supply ground, and the drain is coupled to the magnetoresistive random access memory circuit; and

a positive supply voltage coupled to the magnetoresistive random access memory circuit so as to allow current to flow through the magnetoresistive random access memory circuit when an activation signal is applied to the gate by the control circuit, wherein the control circuit comprises means for regulating a voltage level at the gate, so as to limit the amount of current flowing through the CMOS n-channel transistor and the magnetoresistive random access memory circuit.

12. (Original) The word current source of claim 11 wherein the means for regulating the voltage level comprises a feed back amplifier.

13. (Original) The word current source of claim 11 wherein the control circuit comprises means for regulating a current flowing through the CMOS n-channel transistor when the CMOS n-channel transistor is turned on and off.

14. (Original) The word current source of claim 11 with the control circuit further comprising a stabilization amplifier.

15. (Original) The word current source of claim 14 with the stabilization amplifier further comprising, in combination:

a logic control having a read/write input and an on/off input and a write reference gate control signal and a read reference gate control signal;

a read reference switch having a read reference input and a reference output, with the read reference switch having a read reference control connected to the read reference gate control signal;

a write reference switch having a write reference input and a write reference output connected to the reference output, with the write reference switch having a write reference control connected to the write reference gate control signal; and

a feedback amplifier connected to the reference output, having a mirror current output and a mirror feedback voltage input.

16. (Cancelled).

17. (Currently Amended) ~~The word current source of claim 16~~ A word current source for a magnetoresistive random access memory circuit comprising, in combination:

a control circuit having a control input;

a n-channel semiconductor device including a first terminal, a second terminal and a third terminal, where the first terminal is coupled to a supply ground, and the second terminal is coupled to the magnetoresistive random access memory circuit; and

a positive supply voltage, coupled to the magnetoresistive random access memory circuit so as to allow current to flow through the magnetoresistive random access memory circuit when an activation signal is applied to the third terminal by the control circuit;

wherein the control circuit comprises means for regulating a voltage level at the third terminal, so as to limit the amount of current flowing through the n-channel semiconductor device and the magnetoresistive random access memory circuit.

18. (Original) The word current source of claim 17 wherein the means for regulating the voltage comprises a feed back circuit.

19. (Cancelled).